RCA digital integrated circuits

LOW-POWER COS/MOS* BINARY COUNTER
7-Stage Ripple-Carry Type
Monolithic Silicon

CD4004
CD4004T

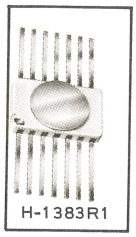
File No. 347

RCA-CD4004 and CD4004T are each comprised of 58 n-channel and 58 p-channel enhancement type MOS transistors connected to form a pulse input-shaping circuit and seven ripple-carry binary counter stages. Resetting the counter to the all 0's state is accomplished by a high-level on the reset line. A master-slave flip-flop configuration is utilized for each counter stage. The state of the counter is advanced one step in binary order on the negative-going transition of the input pulse.

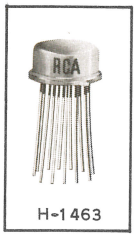
The CD4004 utilizes a hermetically sealed 14-lead "Flat Pack" ceramic-and-metal package (terminals 13 and 14 are not used). The CD4004T is identical electrically and in terminal numbering, and is supplied in a 12-lead TO-5 package. Both types are operable over the full military temperature range of -55°C to +125°C.

7-STAGE COMPLEMENTARY-SYMMETRY MOS BINARY COUNTER

For Digital Circuits in Aerospace and Airborne Computers, Portable Military Equipment, and Instrumentation and Industrial Control Equipment



CD4004



CD4004T

FEATURES

- Logic Block Complexity on a single chip -- each output accessible and resettable
- Static Counter Operation -- counter retains state indefinitely with input pulse level low or high
- Microwatt Quiescent Power Dissipation -- P_T = 5 μW (typ.)
- High Noise Immunity -- 45% of V_{DD} (typ.) over full temperature range
- Operation from single positive or negative power supply -- 6 to 15-volt range
- Large fan-out capability -- > 50 from any output stage
- Fixed logic swing, independent of system and fan-out variation -- V_{DD} to V_{SS}
- Medium Speed Operation -- 2.5 MHz (typ.) input pulse rate with 10-volt supply
- High Input Impedance -- 10^{12} Ω (typ.)
- Low "1"-and "0"-level output impedance -- 2000Ω (typ.) with 10-volt supply

APPLICATIONS

- Digital equipment where low power dissipation and/or high noise immunity are primary design requirements
- Frequency-dividing circuits
- Time-delay circuits
- Counter control

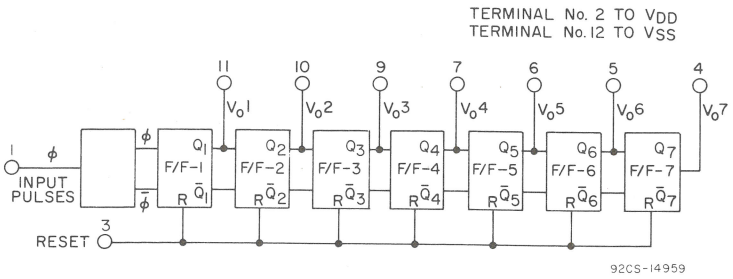


Fig.1 - Functional diagram for CD4004 and CD4004T.

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* Complementary-Symmetry Metal-Oxide-Semiconductor.

ABSOLUTE MAXIMUM LIMITS:

STORAGE-TEMPERATURE RANGE . . . -65°C to +150°C
OPERATING-TEMPERATURE RANGE . -55°C to +125°C
DC SUPPLY VOLTAGE (V_{DD} - V_{SS}) . . . . . +15, -0.5 V
DC CURRENT DRAIN . . . . . 10 mA
ALL INPUTS . . . . . $V_{SS} \leq V_{IN} \leq V_{DD}$
MINIMUM RECOMMENDED POWER SUPPLY VOLTAGE (V_{DD} - V_{SS}) . . . . . 6 V

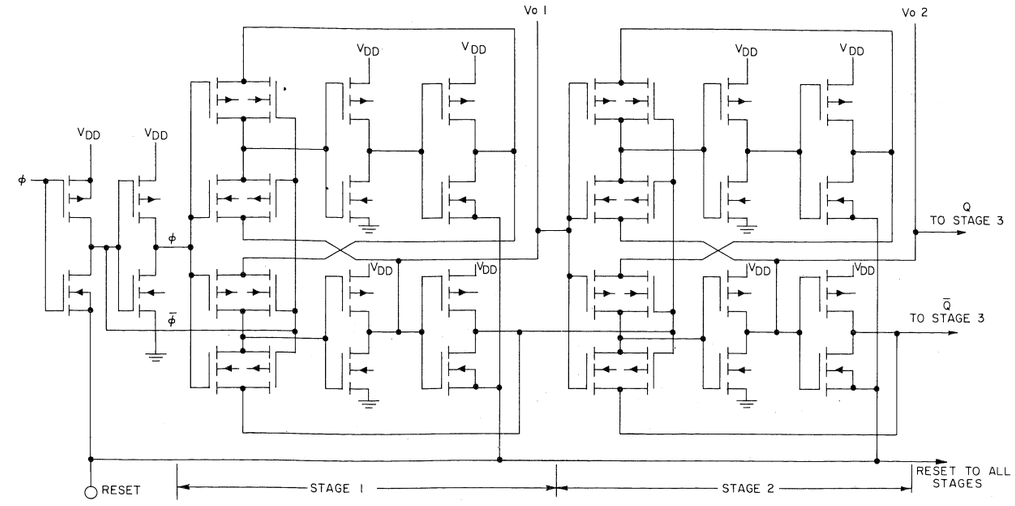
STATIC ELECTRICAL CHARACTERISTICS, at T_A = 25°C, (V_{DD} - V_{SS}) = +10 V, Unless Otherwise Specified.

CHARACTERISTICS	SYMBOLS	WHERE MEASURED	TEST CONDITIONS	LIMITS CD4004 CD4004T MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES AND TEST CIRCUITS FIGS.
"0" Output Voltage	V_{OUT}"0"	Q_{1-7}	Fan-out ≤ 10 MOS Gate Loads — All "0"s	-	0	0.01	V	-
"1" Output Voltage	V_{OUT}"1"		All "1"s	9.99	10	-	V	-
DC Input Current	I_{ϕ}	ϕ	V_{IN} = 0 V	-	10	-	pA	-
			V_{IN} = +10 V	-	10	-	pA	-
Quiescent Device Dissipation Per Package	P_T	-	f_{ϕ} = 0, V_{IN} = 0	-	5	100	μW	7
			f_{ϕ} = 0, V_{IN} = 10 V	-	5	100	μW	
Input Capacitance (Average)	C_{IN}	ϕ		-	3.5	-	pF	12
		Reset		-	40	-	pF	13
Output Drive Capability	I_{DS}"P"	Q_{1-7}	V_{GS} = -10 V, V_{DS} = -2 V	-0.8	-1.3	-	mA	8,9
			V_{GS} = -10 V, V_{DS} = -0.5 V	-0.25	-0.4	-	mA	
	I_{DS}"N"		V_{GS} = 10 V, V_{DS} = 1.5 V	0.8	1.7	-	mA	10,11
			V_{GS} = 10 V, V_{DS} = 0.5 V	0.25	0.55	-	mA	
Reset "Low" Voltage*	V_{Reset}"Low"	-	T_A = -55°C to +125°C, V_{SS} = 0, V_{DD} = 6 V, I_{Reset} = 1 mA	-	-	0.2	V	-
			T_A = -55°C to +125°C, V_{SS} = 0, V_{DD} = 10 V, I_{Reset} = 2 mA	-	.	1	V	-
			T_A = -55°C to +125°C, V_{SS} = 0, V_{DD} = 14 V, I_{Reset} = 4 mA	-	-	2	V	-
Threshold Voltage: ϕ	$V_{TH(\phi)}$	-	Typical Threshold Voltage Temperature Coefficient = -2 mV/°C, V_{SS} = 0 V, V_{DD} = 6 V	1.4	3	4.5	V	4,5
			V_{DD} = 10 V	3.3	4.5	6.7	V	
			V_{DD} = 14 V	4.5	6	9.7	V	
Reset	V_{TH}Reset	-	V_{DD} = 6 V	1.0	4	5.5	V	6
			V_{DD} = 10 V	2.5	5	6.7	V	
			V_{DD} = 14 V	4.5	6.5	9.7	V	

* Reset line drive impedance must be such that the specified conditions are met. For example, with V_{DD} = 10 V the reset line voltage must not exceed 1 volt. For a typical peak current of 2 mA this requires that the drive impedance be ≤ 500 Ω.

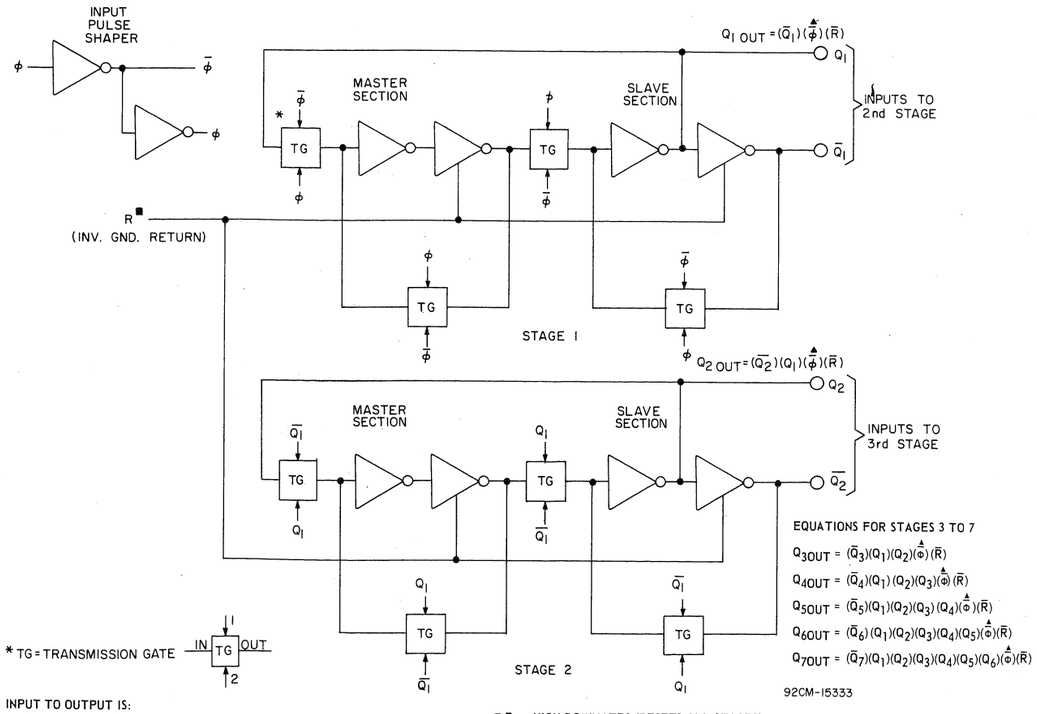
DYNAMIC ELECTRICAL CHARACTERISTICS, at T_A = 25°C, V_{SS} = 0 V, Typical Temperature Coefficient = +0.3%/°C (-0.3%/°C for fΦ).

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS CD4004 CD4004T MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES AND TEST CIRCUITS FIGS.
"0" Propagation Delay	t_{pd0}	C_{Q1}-C_{Q7} = 30 pF	V_{DD} = +6 V	-	550	-	ns	14a,14b,14c
			V_{DD} = +10 V	-	175	400	ns	
			V_{DD} = +14 V	-	110	-	ns	
"1" Propagation Delay	t_{pd1}		V_{DD} = +6 V	-	600	-	ns	14a,14b,14d
			V_{DD} = +10 V	-	190	400	ns	
			V_{DD} = +14 V	-	120	-	ns	
"0" Transition Time	t_0		V_{DD} = +6 V	-	400	-	ns	14a,14b,14e
			V_{DD} = +10 V	-	150	350	ns	
			V_{DD} = +14 V	-	110	-	ns	
"1" Transition Time	t_1		V_{DD} = +6 V	-	620	-	ns	14a,14b,14f
			V_{DD} = +10 V	-	225	450	ns	
			V_{DD} = +14 V	-	150	-	ns	
"0" Input-Pulse Duration	$t_w\bar{\phi}$		V_{DD} = +6 V	2000	-	-	ns	14a,14g
			V_{DD} = +10 V	600	-	-	ns	
			V_{DD} = +14 V	400	-	-	ns	
"1" Input-Pulse Duration	$t_w\phi$		V_{DD} = +6 V	500	-	-	ns	
			V_{DD} = +10 V	200	-	-	ns	
			V_{DD} = +14 V	100	-	-	ns	
Input-Pulse Frequency $\left(f_{\phi} = \frac{1}{t_w\bar{\phi} + t_w\phi}\right)$	f_{ϕ}		V_{DD} = +6 V	-	-	0.4	MHz	
			V_{DD} = +10 V	-	-	1.25	MHz	
			V_{DD} = +14 V	-	-	2	MHz	
Input-Pulse Rise and Fall Times	$t_{r\phi} = t_{f\phi}$	C_{Q1}-C_{Q7} = 30 pF, T_A = -55°C to +125°C	V_{DD} = +6 V	-	-	15	μs	14a,14h
			V_{DD} = +10 V	-	-	15	μs	
			V_{DD} = +14 V	-	-	15	μs	
Reset Propagation Delay Time	t_{pd}Reset	C_{Q1}-C_{Q7} = 30 pF	V_{DD} = +6 V	-	500	1650	ns	15a,15b
			V_{DD} = +10 V	-	80	400	ns	
			V_{DD} = +14 V	-	50	200	ns	
Reset-Pulse Duration	t_wReset		V_{DD} = +6 V	1650	-	-	ns	
			V_{DD} = +10 V	400	-	-	ns	
			V_{DD} = +14 V	200	-	-	ns	



NOTE: SUBSTRATES FOR ALL "P" UNITS ARE CONNECTED TO V_{DD}
SUBSTRATES FOR ALL "N" UNITS, UNLESS OTHERWISE SHOWN, ARE CONNECTED TO GROUND.

Fig.2 - Schematic diagram of pulse shaper and two (of seven) binary stages of the CD4004 and CD4004T.



* TG = TRANSMISSION GATE

INPUT TO OUTPUT IS:
a) A BIDIRECTIONAL SHORT CIRCUIT WHEN CONTROL INPUT 1 IS "LOW" AND CONTROL INPUT 2 IS "HIGH".
b) AN OPEN CIRCUIT WHEN CONTROL INPUT 1 IS "HIGH" AND CONTROL INPUT 2 IS "LOW".

EQUATIONS FOR STAGES 3 TO 7

$Q_{3OUT} = (\bar{Q}_3)(Q_1)(Q_2)(\overset{\blacktriangle}{\bar{\phi}})(\bar{R})$

$Q_{4OUT} = (\bar{Q}_4)(Q_1)(Q_2)(Q_3)(\overset{\blacktriangle}{\bar{\phi}})(\bar{R})$

$Q_{5OUT} = (\bar{Q}_5)(Q_1)(Q_2)(Q_3)(Q_4)(\overset{\blacktriangle}{\bar{\phi}})(\bar{R})$

$Q_{6OUT} = (\bar{Q}_6)(Q_1)(Q_2)(Q_3)(Q_4)(Q_5)(\overset{\blacktriangle}{\bar{\phi}})(\bar{R})$

$Q_{7OUT} = (\bar{Q}_7)(Q_1)(Q_2)(Q_3)(Q_4)(Q_5)(Q_6)(\overset{\blacktriangle}{\bar{\phi}})(\bar{R})$

■ R = HIGH DOMINATES (RESETS ALL STAGES).

▲ ACTION OCCURS ON NEGATIVE GOING TRANSITION OF INPUT PULSE. COUNTER ADVANCES ONE BINARY COUNT ON EACH NEGATIVE Φ TRANSITION (128 TOTAL BINARY COUNTS).

Fig.3 - Logic block diagram and equations for input pulse shaper and two (of seven) binary stages of the CD4004 and CD4004T.

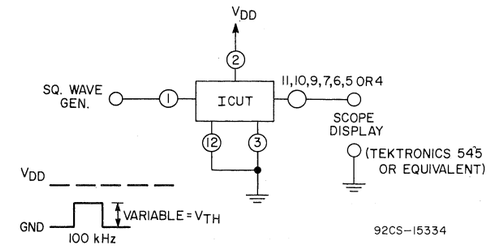


Fig.4 - Input pulse threshold test circuit—master section changing (input low-to-high transition).

TEST PROCEDURE:

1. Slowly raise input-pulse amplitude until counter stage output begins to switch.
2. Pulse amplitude equals threshold voltage.

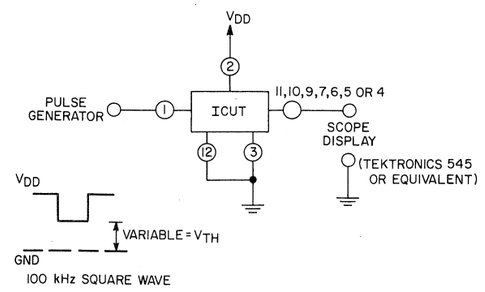


Fig.5 - Input pulse threshold test circuit—slave section changing (input high-to-low transition).

TEST PROCEDURE:

1. Set pulse base line to V_{DD} value.
2. Slowly increase negative pulse amplitude until counter stage output begins to switch.
3. Ground to most negative pulse level equals the threshold voltage.

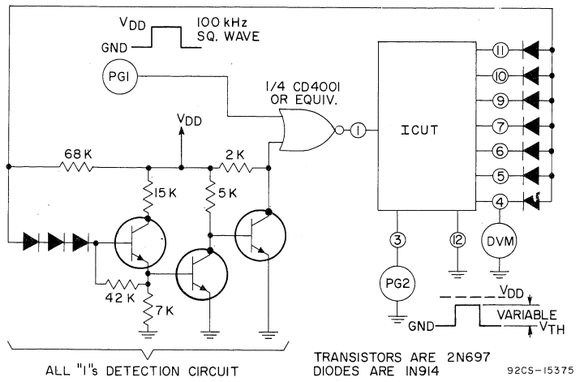


Fig.6 - Reset-line threshold test circuit.

TEST PROCEDURE:

1. Run counter to all "1"s state with pulse generator No.1 --- detection circuit stops input pulses at all "1"s state.
2. Slowly raise pulse amplitude on RESET line (pulse generator No.2) until counter stage output goes to "0" state.

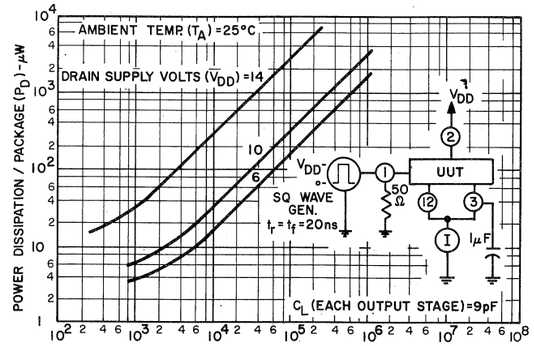


Fig.7 - Typical dissipation characteristics.

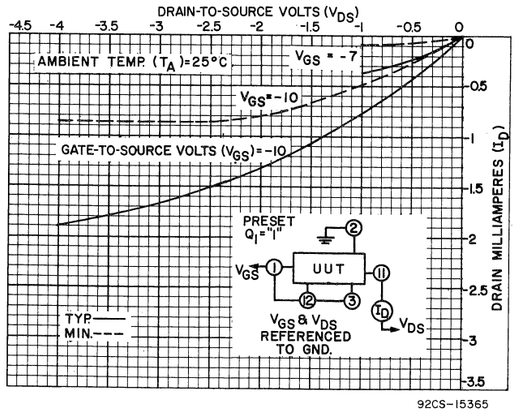


Fig.8 - Minimum and typical p-channel device output drive characteristics as a function of V_{GS}.

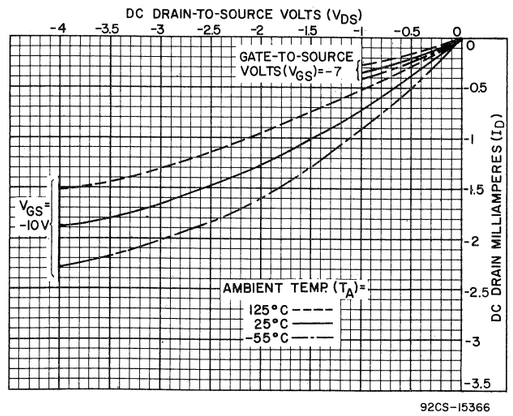


Fig.9 - Typical p-channel device output drive characteristics as a function of temperature.

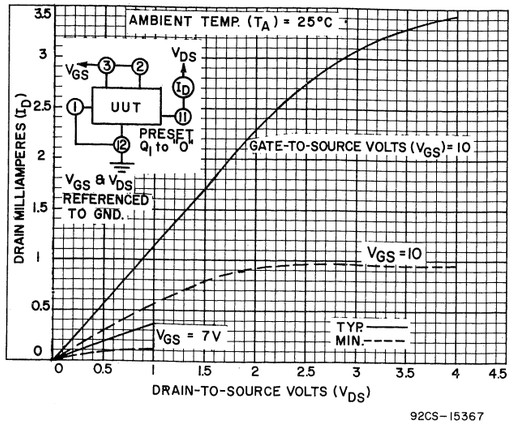


Fig.10 - Minimum and typical n-channel device output drive characteristics as a function of V_{GS}.

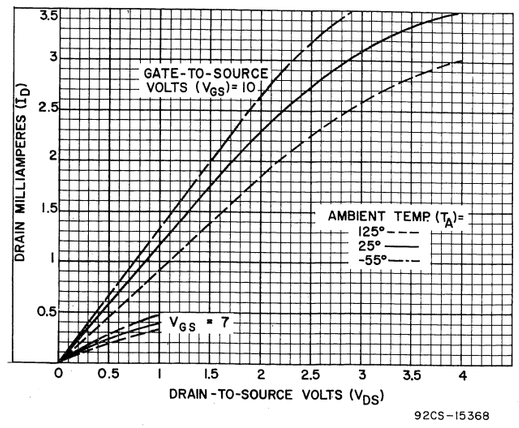


Fig.11 - Typical n-channel device output drive characteristics as a function of temperature.

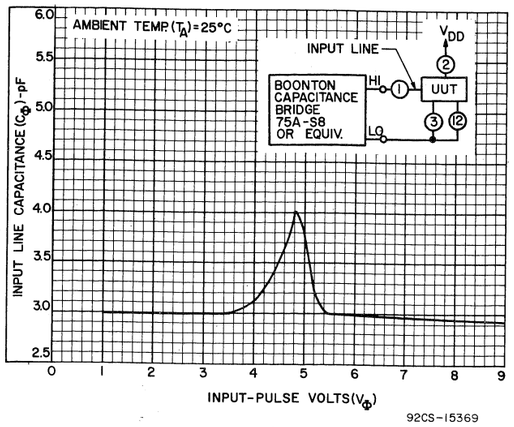


Fig.12 - Typical input capacitance characteristic.

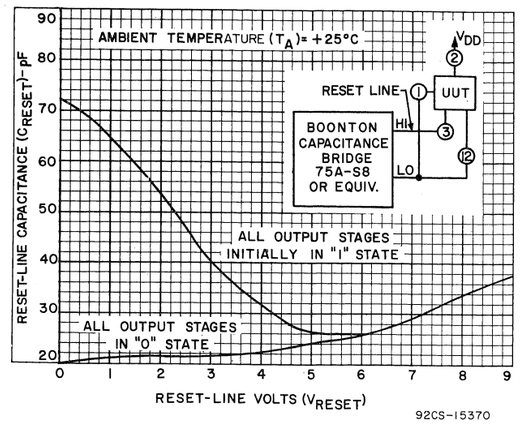


Fig.13 - Typical reset-line capacitance characteristics.

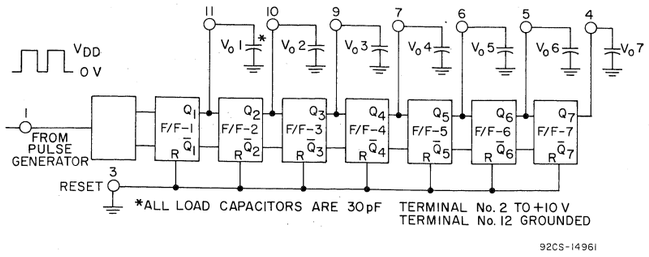


Fig.14a - Dynamic input-pulse characteristics test setup.

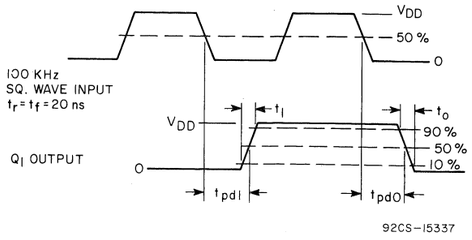


Fig.14b - Waveforms for measurement of propagation delay and transition times.

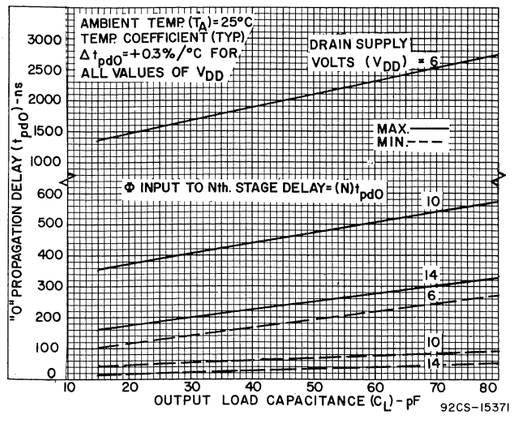


Fig.14c - "0" propagation delay characteristics.

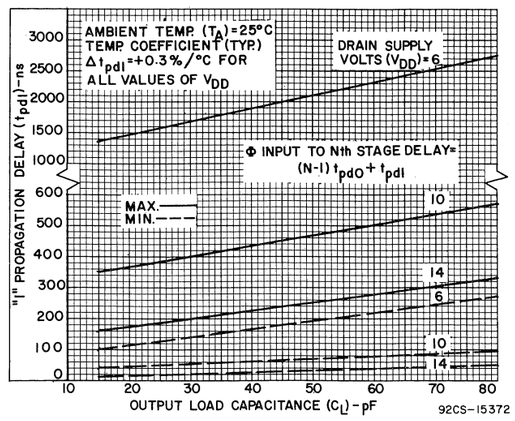


Fig.14d - "1" propagation delay characteristics.

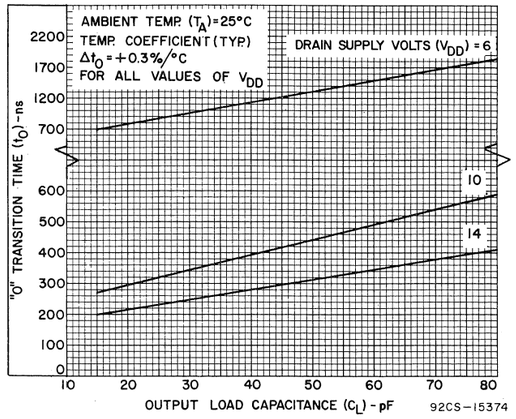


Fig.14e - Maximum "0" transition time characteristics.

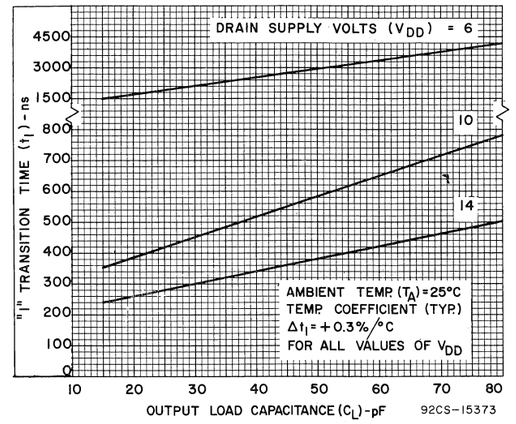


Fig.14f - Maximum "1" transition time characteristics.

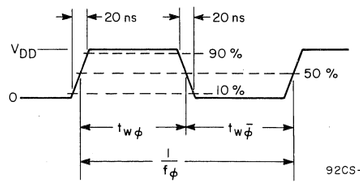


Fig.14g - Waveform for measurement of minimum input-pulse durations and maximum input-pulse frequency.

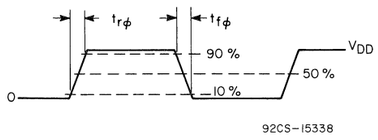


Fig.14h - Waveforms for measurement of maximum input-pulse rise and fall times.

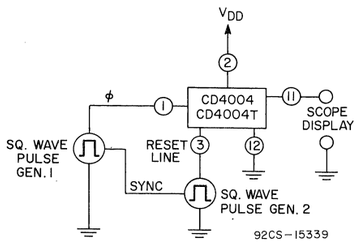


Fig.15a - Dynamic characteristics test setup for reset-pulse measurement.

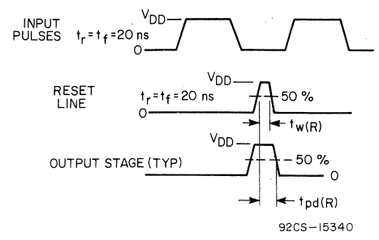


Fig.15b - Waveforms for measurement of reset propagation delay and minimum reset-pulse duration.

OPERATING CONSIDERATIONS

The leads of these devices are usually soldered to external circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the device against high electric fields. Although a certain degree of protection against such fields is provided by built-in circuitry, it is recommended that this device not be inserted in conventional plastic "snow" or plastic trays of the types frequently used for the storage and transportation of small semiconductor devices.

These units should not be connected into, or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the device. All unused input leads should be connected to the most negative circuit potential. It is recommended that low impedance pulse generators or power supplies connected to the inputs of this device be removed before the power supply is turned off. This precaution will prevent the signal on the gate from exceeding the power supply voltage and thus prevent possible damage to the protective circuitry.

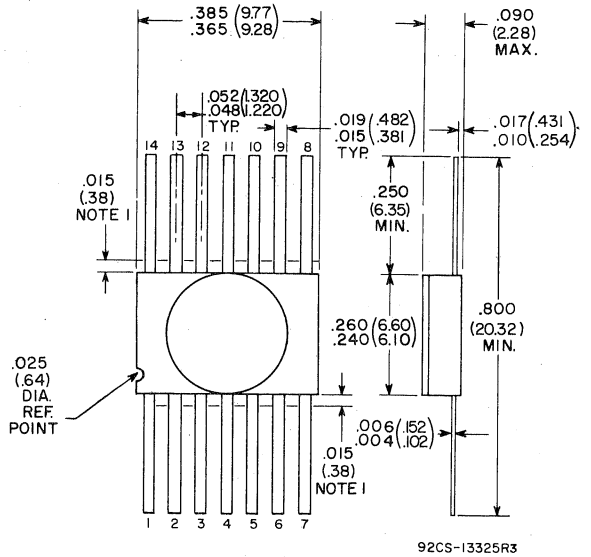
DIMENSIONAL OUTLINES

Dimensions in Inches and Millimeters

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.

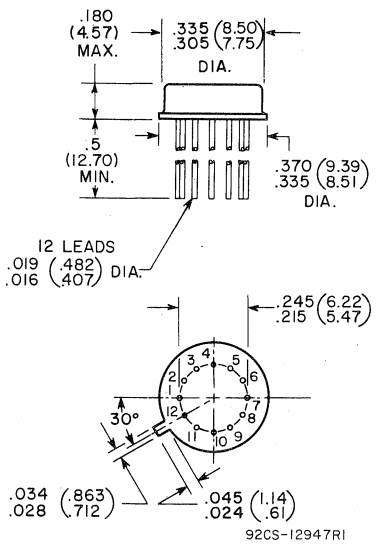
CD4004

14-LEAD FLAT PACK



CD4004T

12-LEAD TO-5 STYLE



Note 1: Lead dimensions in this zone are not controlled because of irregularities in body and lead finish.

Lead spacing shall be measuren within 0.030 inch (.762 mm) from the point of emergence from the body.